Front-End Electronics for PHENIX Time Expansion Chamber

K. Barish, W. C. Chang, O. Dietzsch, T. Ferdousi, A. Franz, J. Fried, S. Y. Fung, J. Gannon, J. Harder, A. Kandasamy, M. A. Kelley, D. Kotchetkov, A. Lebedev, X. H. Li, J. Mahon, S. Mioduszewski, M. Muniruzzaman, B. Nandi, E. O'Brien, P. O'Connor, R. Pisani, S. Rankowitz, M. Rosati, R. Seto, E. M. Takagui, W. Von Achen, H. Q. Wang, and W. Xie

Abstract—Front-end electronics (FEE) has been developed for the PHENIX time expansion chamber (TEC), a multiwire tracking detector with over 20k readout channels. The FEE for the TEC consists of an analog preamplifier-shaping amplifier circuit board, a digital front-end module circuit board plus ancillary support boards for timing, control and communication. Signals from each chamber wire are sampled ($\sim$40 MHz), digitized, buffered, and then formatted as 64 channel serial data packets to be transmitted via a 1-GHz optical link. Three custom ICs have been designed for this system: 1) octal preamplifier and shaping amplifier with tail cancellation and dual-gain for large dynamic range with full serial control of gain, shaping time and tail; 2) nonlinear 5-b flash ADC with 9-b dynamic range; 3) digital memory unit for programmable delay and memory depth. The FEE has been installed, commissioned, and operated in the PHENIX experiment at Brookhaven National Laboratory.

Index Terms—Front-end module, preamplifier/shaper, TEC.

Fig. 1. The TEC electronics chain.

I. INTRODUCTION

THE time expansion chamber (TEC) is one of the main tracking detectors in the PHENIX experiment at the Relativistic Heavy Ion Collider (RHIC) located at Brookhaven National Laboratory [1]. RHIC will collide ions ranging from protons to gold nuclei (including dissimilar species) at center of mass energies up to 200 GeV/nucleon. The TEC performs tracking functions and identifies particles by sampling their ionization energy loss (dE/dx) and by detecting associated transition radiation (TR) photons [2]. Special front-end electronics (FEE) was developed for the TEC that operates in a diverse experimental environment including two extreme configurations such as Au–Au collisions with high particle-multiplicities and proton–proton collisions with
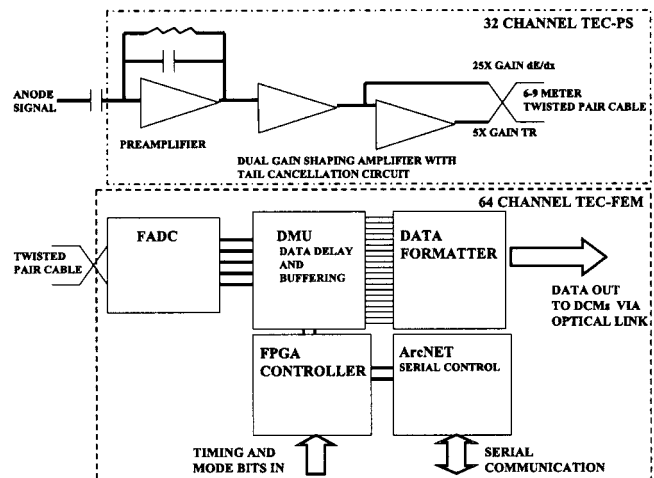
high rates, as well as intermediate configurations for proton and light-ion collisions. Each anode wire is read through a preamplifier/shaping amplifier (P/S) and then digitized to determine the time profile and the pulse height of the signal. Fig. 1 describes the TEC electronics chain.

II. ELECTRONICS REQUIREMENTS

The chambers are composed of a Cu-mylar drift cathode, a 3-cm drift space, and a 6-mm-thick proportional region containing two cathode wire planes surrounding a plane of 25-μm Au-W anode wires [2]. The TEC operates with either a 90–10 argon–ethane (P-10) gas mixture, which has a drift velocity of 25 mm/μ, or a xenon-based mixture with a drift velocity of $\sim$15 mm/μs.

To be simultaneously sensitive to dE/dx and TR events, a dual-gain system is required. According to design specifications, minimum ionizing particles deposit about 0.16 keV/mm in the gas, which corresponds to 8 fC of charge into the preamplifier per time bucket (25 ns). For this input signal, adequate electron–pion separation can be achieved with an equivalent input noise charge (ENC) of 1500 rms electrons. The analog electronics must not saturate when the charge associated with a 10-keV (300 fC) TR photon is received at the preamp in 100 ns or less.

The maximum average level-1 trigger rate is designed as 25 kHz for the PHENIX experiment while the frequency of
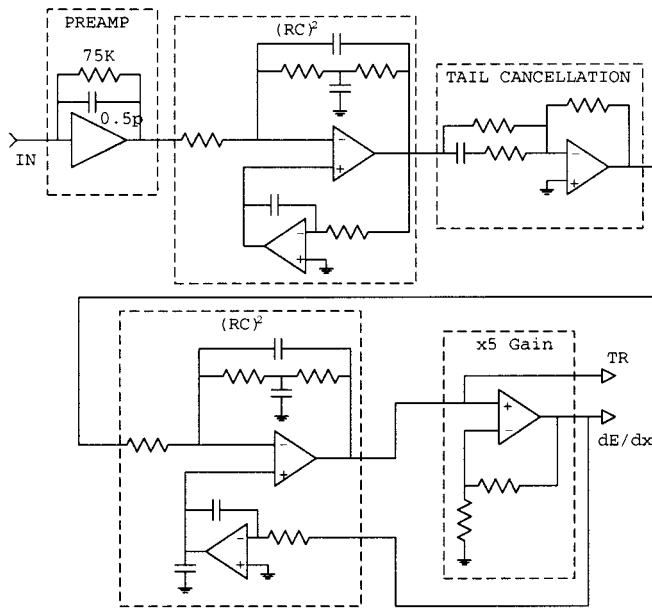
Fig. 2.   Block diagram of the P/S chip.

beam collision is 9.4 MHz at the RHIC. This requires a fast operation of the TEC FEE.

III. A MONOLITHIC PREAMPLIFIER/SHAPER

A P/S chip (Fig. 2) has been implemented in an octal integrated circuit. The chip is described in detail elsewhere [3]. It incorporates a 75-kΩ transimpedance preamplifier, a two-bridged-T type shaping amplifier with semi-Gaussian CR-RC^4 shaping, an ion tail cancellation stage, and an output gain stage. Each stage has digitally controlled capacitor and resistor arrays to adjust time constants and gain ratios.

Since the entire preamplifier is dc coupled, offsets are controlled using two active feedback loops with long time constants. A first stage of shaping is implemented to eliminate the need of an additional preamp tail cancellation. Each channel has an on-chip charge injection capacitor of 0.5 pF that can be switched into or out of the circuit to use in calibration. In addition, there is an on-chip disable switch that allows noisy channel to be switched off.

The shaping amplifier chain has a shaping time of 70 ns. It allows the flash-ADC clock to run at a fraction of the shaping time to achieve good position resolution and also for the total signal from the TR X-rays to be absorbed by the gas chamber. A variable tail cancellation stage has been realized in the shaping amplifier chain allowing the electronics to be used in a variety of gas mixtures with different ion mobilities. The signal of the shaper provides a low-gain output sensitive to the TR signals. A noninverting active gain stage provides a fixed gain of 5 for the dE/dx output.

A 24-b shift register stores configurations in serial link. There are 3 b used for gain tuning, 3 b for tail cancellation settings, and 2 b for shaping time settings. Another 16 b are used for the masks of calibration and read-enable of the 8 channels in the P/S chip. The masks are controlled for each channel whereas the other settings are global for the entire P/S chip. These features serve as a major diagnostic tool for the circuit and the detector.
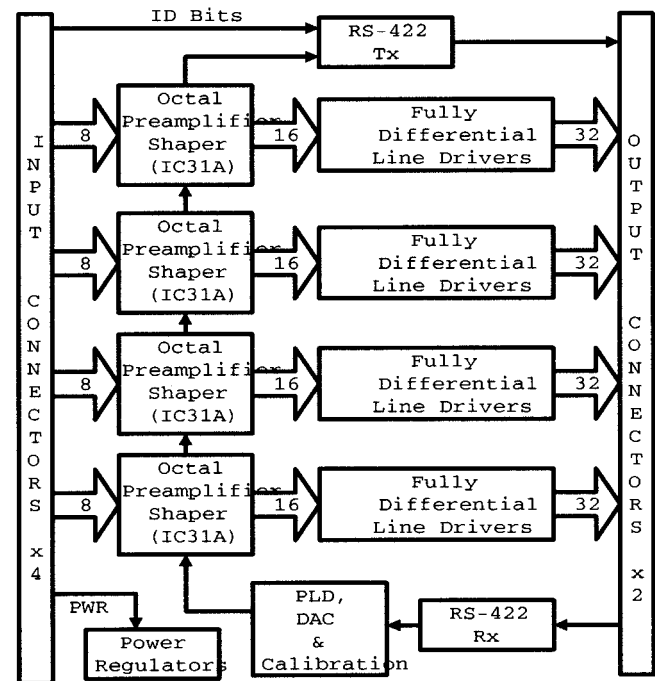

Fig. 3.   Thirty-two channel preamplifier/shaping amplifier board.

The block diagram of the P/S board is shown in Fig. 3. Four octal P/S chips are daisy chained using their serial lines, such that the configuration data can be downloaded in a single data stream. Operational amplifiers are used as differential line drivers for output signals. A digital-to-analog converter (DAC) provides reference voltage for calibrating the 32 P/S channels. It is set using a serial stream downloaded to the programmable logic device (PLD). Local low-drop-out regulators regulate onboard power and supply filtering circuits. Poly-resettable fuses protect against excess current. External electrostatic discharge (ESD) protection for preamplifier input is realized with resistors and two pull-up and pull-down diodes.

A single data stream of 108 b, 96 for the P/S chips and 12 for the calibration DAC, and a calibration strobe are received over the twisted pair cable from the front-end module (FEM) as differential RS-422 level signals. The data stream can be read back for verification with RS-422 signaling.

Each FEM is connected to two 32-channel P/S boards for a total of 64 channels. Each channel is further subdivided into separate dE/dx and TR signal pairs, giving a total of 128 twisted pairs. These analog signals are routed from the input connectors to differential line receivers and then to flash-ADC chips, where the signals are digitized.

IV. FLASH-ADC

A 37.7-MHz, custom analog-to-digital converter (ADC) [4] has been designed for the TEC FEE. The chip consists of two individual flash ADCs having a common digital encoder that produces a single 5-b binary coded output with 9-b dynamic range (Fig. 4). The flash-ADC receives two outputs of a single P/S channel, the high gain ($\times 5$) dE/dx and the low gain ($\times 1$) TR. In this way, signal ranges are set to match the dynamic ranges of the flash-ADC inputs. Optimum resolution is, therefore, main-
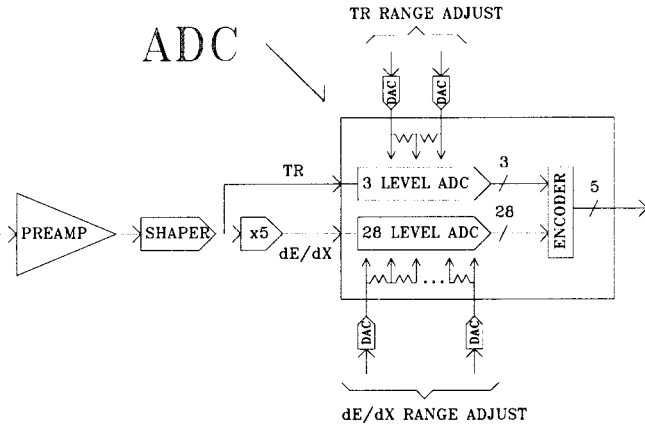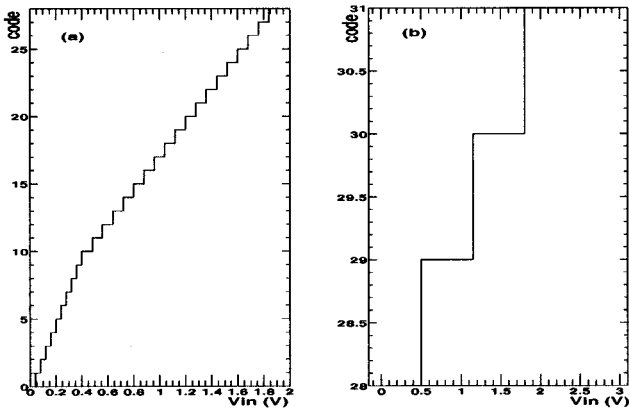
Fig. 4. Block diagram of the TEC flash-ADC.

Fig. 6. Block diagram of the TEC DMU.

Fig. 5. Transfer functions of the TEC flash-ADC. (a) The dE/dx input. (b) The TR input.

tained over a large dynamic range without the need for many high precision comparators. Fig. 5(a) shows the output of the dE/dx input which has two linear segments to increase dynamic range. The first segment covers codes 0–10 and has a slope of one least significant bit (LSB) per 40 mV. The second segment covers codes 11–28 and has a slope of 1 LSB per 80 mV. The resolution is highest for small signals because this is the region where the best discrimination between electrons and pions is realized. Fig. 5(b) shows codes 29–31 with respect to only large input signals which are expected to be produced by the TR photons. The slope in this graph is 1 LSB per 650 mV. The chip is a 24-pin SSOP package based on a 1.2-μm CMOS process.

Each internal ADC contains a resistor chain that generates the voltage levels at which corresponding comparators switch (Fig. 4). Both ends of the chains are brought out to pins so that their endpoint voltages may be adjusted by external sources such as programmable DACs. This permits the user to set the transfer functions of each ADC.

V. DIGITAL MEMORY UNIT

The digital memory unit (DMU) (Fig. 6) is a custom IC that receives the digitized data on four channels from Flash-ADCs. The DMU performs two functions: 1) the level–1 delay and 2)
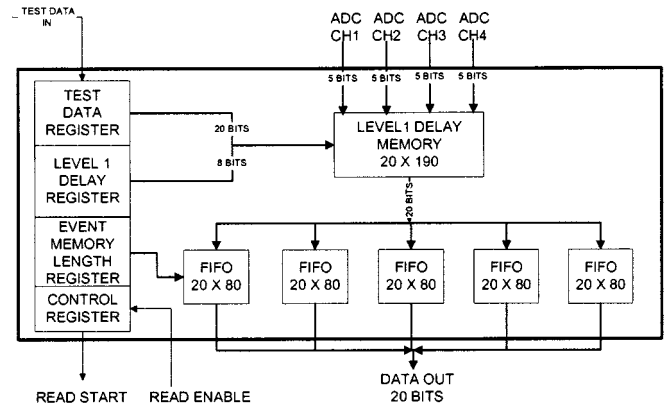
the event memories that store data until the reformatter can accept them. The DMU also contains a test data register which provides a test pattern for testing, and a control register. The DMU is a 24-b device; however, since we only use 20 b, most of the following description deals with only 20 b.

The control register performs four functions: loading test data to the test data register; gating real data or test data to the level-1 delay memory; setting the level-1 delay; setting the event memory length.

The level-1 delay memory is a first-in–first-out memory (FIFO). The length of the FIFO is set by the level-1 delay register. The maximum length is 190 time buckets. The level-1 delay memory works in the following manner. The first data word after the system has been powered up is asserted on the input pins of the level-1 delay memory. This data word immediately appears on the output pins. All subsequent input data pile up behind the first word. When the FIFO is full, the next word written on the input causes the word on the output to shift out. This way we create a circular buffer to save data while the level-1 accept is being generated. With the presence of the level-1 accept, the words that have been shifted out are accepted by the event memory. Otherwise, they are simply lost.

Event memories are FIFOs that can store data of $80 \times 4 \times 5$ (*buckets* $\times$ *channels* $\times$ *events*) samples. The length of the event memory is set by the event memory length register. As data are circulating through the level-1 delay memory, they also appear on the event memory inputs. When a level-1 accept arrives at the DMU, the data from the level-1 delay memory are written to one event memory. The event memory selection pointer now is updated to point to the next available event memory that is empty. The writing action continues until the event memory is full. We now wait for the next level-1 accept to start filling the next event memory. If another level-1 accept is received by the DMU while one event memory is being written, writing into the next available event memory is started while the first event memory continues to be written. If all event memories are full and a level-1 accept is received, the error pin on the DMU is asserted. As the event memories are written, the number of the current event memory is asserted on three output pins of the DMU. When an event memory is full and the read-enable pin on the DMU is not asserted, the event memories wait to be read until the read-enable pin is asserted. Upon assertion of the read-
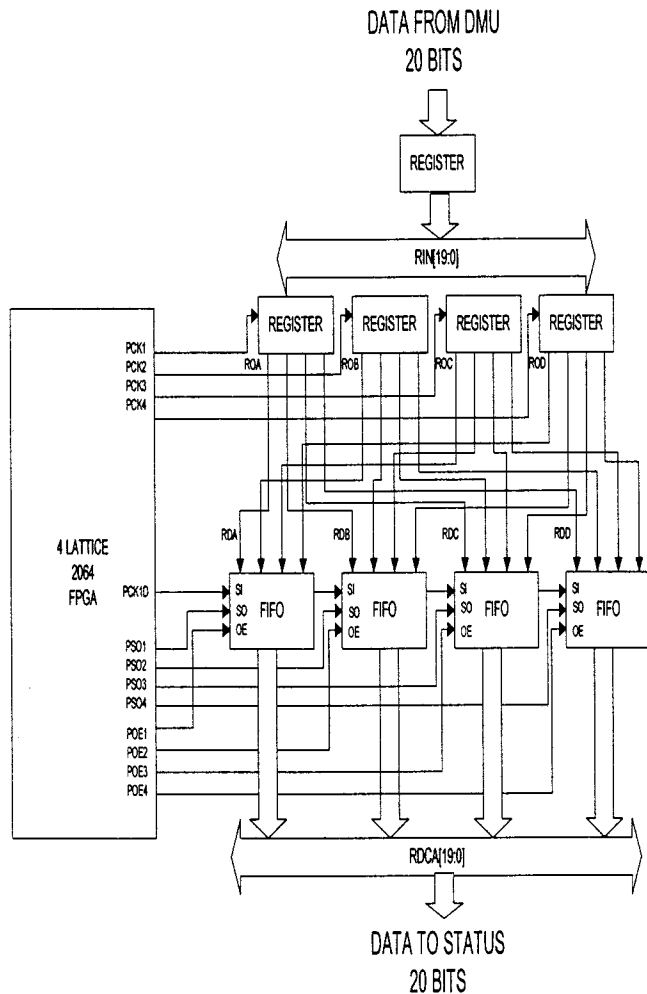
Fig. 7. Block diagram of the TEC data reformatter. PCK: package; SI: shift in; SO: shift out; OE: output enable; and FPGA: field programmable gate array. ROA is a signal name, as well as ROB, RDA, etc.

enable pin on the DMU, reading is started from the next event memory that is full. The start-to-read pin on the DMU is asserted to indicate the start of a read cycle. On every clock asserted on the DMU, a data word is asserted on the DMU data out pins. This output sequence continues until the event memory is empty.

VI. DATA REFORMATTER

The reformatter accepts data from the DMU output. It then rearranges them to a format that the PHENIX data collection module (DCM) [5] can accept. Fig. 7 is a hardware oriented diagram of the way the data are reformatted. Each 20-b sample from the DMU is composed of 4 channels. Upon receipt of a start-to-read signal from a DMU, the reformatter starts reading the DMU. The reading process starts from the first DMU. When all samples are read from the first DMU, the second DMU is asserted. This sequence continues until all 16 DMUs (64 channels) are read. Upon entry, the 20-b word contains one sample from each of four channels. The following actions are taken at sequential clock tics: these samples are clocked into register A; second, third, and fourth samples from channels 1–4 are clocked into registers B, C, and D, respectively; fifth samples from channels 1–4 are clocked into the register A and the data samples
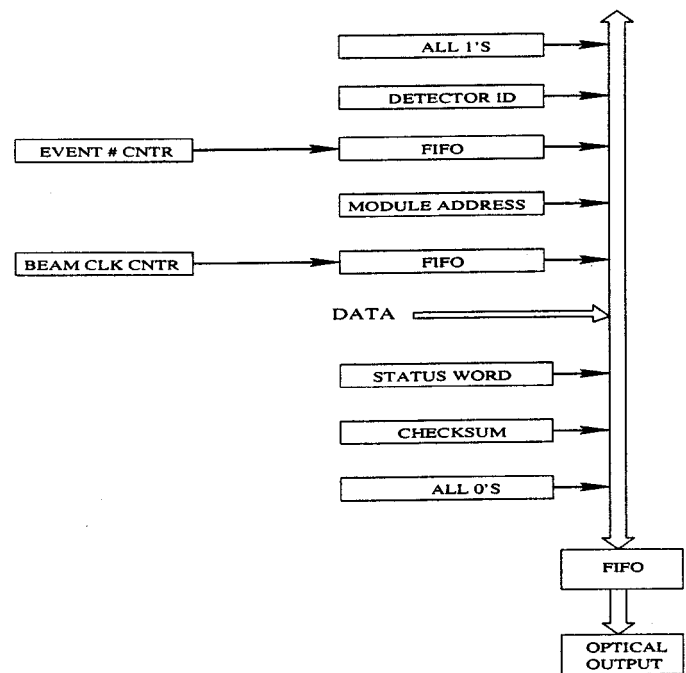

Fig. 8. TEC status and control words.

contained in the registers A, B, C, and D are clocked into FIFO A, B, C, and D. As data are clocked from the register to the FIFO they are reformatted. Register A contains one sample from the 4 channels. After clocking into the FIFO, FIFOs A, B, C, and D contains four samples from the channels 1, 2, 3, and 4, respectively. This sequence continues until the required number of samples are clocked into the FIFOs. After FIFO A has been filled with the required number of samples, the formatter starts clocking it out. After this process has been completed, the formatter starts clocking out FIFO B. This sequence continues until all samples are clocked out into the output. While the formatter is clocking data out of the FIFOs, the clocking data into Registers A, B, C, and D continues until all DMUs are empty.

Before data from the reformatter leave the FEM, status and control words are added to the data stream (Fig. 8). These words indicate the start and the end of the data stream, the module address, the level-1 counter, the beam-crossing counter, and the longitudinal check-sum. These informations serve diagnostic tools in experiment.

Formatted data are transmitted over a Giga-link (Hewlett Packard HDMP-1012) to the DCM which performs zero suppression and error checking.

VII. ANCILLARY SUPPORT BOARDS

A Giga-link receiver card on the time interface card (TIC) (Fig. 9) accepts the 20 timing and control bits driven by the PHENIX granule timing module (GTM) [6] through an optical fiber link at four times the beam clock (BeamClkX4, or 37.7 MHz). This signal is driven to the FEMs as an accurate timing reference. The beam clock signal provides phase information for the BeamClkX4 signal and also indicates the beam crossing. A number of control signals including the module address, the node address for remote serial control, the mode control signal and the endat signal are distributed to backplane
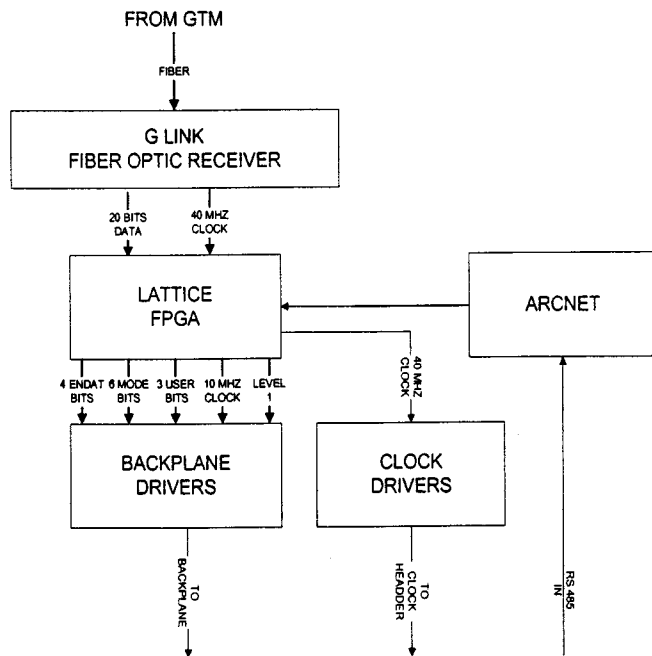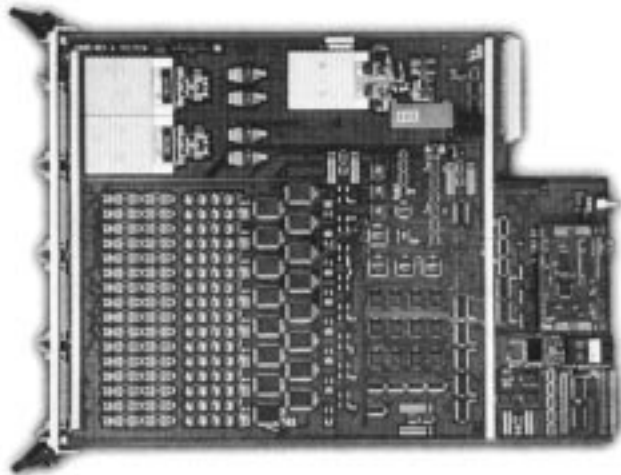
Fig. 9. Block diagram of the TEC TIC.

Fig. 10. TEC FEM.

and received by the FEMs. Endats 1–4 are used to control which FEM is to be read out next. The TIC also synchronously resets the level-1 counter in all FEMs in serial control.

The PHENIX Arcnet daughter card[1] is used for serial communication with the FEE.

Fig. 10 shows a picture of a TEC FEM.

VIII. Testing and Performance

For a system of this size, testing is a major issue. We have built custom testers for both the custom ICs and the FEE boards.

The P/S chip is tested using an automated test fixture which consists of a set of multiplexers to test the bias line and the power supply voltage of the chip, as well as the pulse height, the dc voltage, the pulsewidth, and susceptibility to the ESD of

[1]For more information on Arcnet, see http://www.inst.bnl.gov/~jfried/ar-cnet/arcnet.html
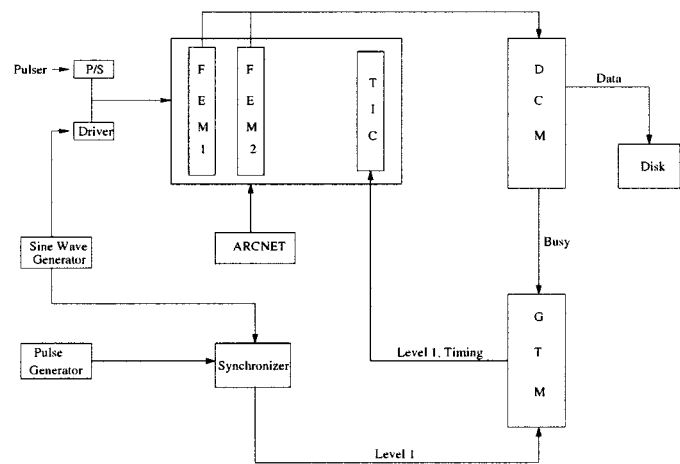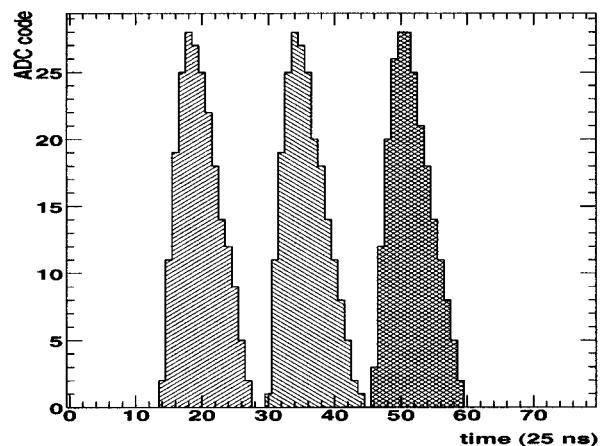

Fig. 11. TEC FEE chain test setup.

Fig. 12. Impulse responses of an FEE channel to three timing settings.

each chip's channel. The ESD test was performed by exciting the inputs of the preamplifier with 100 μJ of energy at a rate of 1 Hz. With an external protection network, the chip sustained over 1000 discharges without failure.

Tests of the TEC P/S chip find the measured integral nonlinearity (INL) is less than 1% for dE/dx and less than 3% for the TR. A channel in the P/S board has less than 2% cross talk with its neighbors.

The Flash-ADC chip is tested using another automated test fixture. The hardware is interfaced to a data acquisition system. The output is measured by using an oscilloscope. The operating range is up to 80 °C ambient temperature and 50 MHz sampling rate. The INL is +0.03 LSB rms for the dE/dx input and better than −0.004 LSB for the TR input.

The TEC FEE is tested in a chain (Fig. 11) that consists of a mini-DAQ developed at the PHENIX experiment [1]. The GTM provides low jitter generation and distribution of timing signals. It also delivers readout-enable strobes. The DCM receives data from the FEMs and sends its busy signal to the GTM which disables further level-1 triggers. The GTM and the DCM are interfaced to separate VME buses. In one test mode, the GTM sends an internal strobe to the TIC which passes it on to the FEMs and triggers calibration pulse in every P/S channel. Fig. 12 shows the responses of one channel to three level-1 delay settings with an
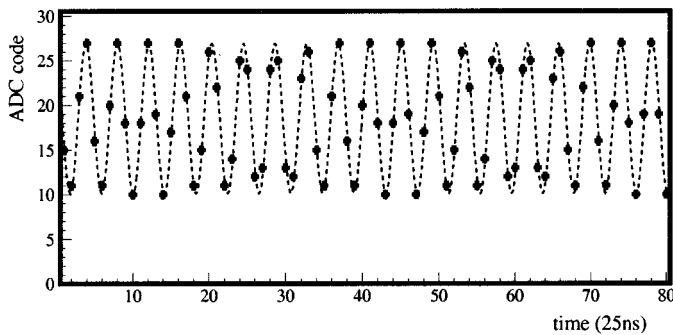
Fig. 13.   Response to a sine wave.

interval of 16 time buckets which is matched in the readout. In the other test mode, a synchronized signal of a pulse and a sine wave is sent to the GTM as the level-1 signal. The sine wave is also used as an analog input signal. Fig. 13 demonstrates a matching between an analog 9.7-MHz sine wave input (dash line) and the digitized FEE readout.

The electronic noise associated with the detector was carefully studied. An individual chamber in the laboratory obtained a noise value of 0.3 fC/channel rms which is close to the ENC of the P/S chip alone. The electronics noise with the full system operating on the PHENIX carriage has an average noise/channel of 1–2 fC rms which is dominated by coherent noise. The noise is within the design specifications of the system.

IX. SYSTEM ISSUES

Considerable effort has gone into the system design of the TEC electronics, with the goal of reducing pick-up noise and eliminating ground loops. All signals from the P/S board are sent differentially. Power supplies are isolated from ground and utilize both active and passive filtering. All grounds (detector, power supply, the P/S, and the FEM) were left isolated until the system was fully installed. Once assembled, the grounds were connected and optimized to reduce noise and ground loops.

A group of 20 FEMs is mounted in a single crate. Temperature fluctuations from FEM to FEM are minimized throughout the crate through the use of rack-mounted fans and heat exchangers connected to a circulating, temperature-controlled chilled water system.

The TEC FEE system has significant diagnostic and error checking capability, remote communication and a complete geographic event readout to check the cabling. These features maintains easy commission and stable operation.

X. CONCLUSION

Custom electronics for measurements of energy loss and transition radiation have been developed for the TEC with over 20k readout channels. Three types of custom chips have been designed and fabricated. Five hundred 32-channel P/S boards using octal P/S chips have been fabricated. Two hundred forty 64-channel FEMs equipped with Flash-ADC chips and the DMU chips have been built together with 10 TICs. The TEC electronics has been installed, commissioned and operated in the year-1 PHENIX experiment at Brookhaven National Laboratory for measuring energy loss. It works to specifications. It will be commissioned and operated in the year following the PHENIX experiment for reading out both energy loss and transition radiation.

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